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SHA hash dual core

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An fpga based sha-256 processor

KK Ting, SCL Yuen, KH Lee, PHW Leong - Lecture notes in computer science, 2002 - Springer

 ... Message Scheduler **SHA-256 CORE Dual** Port Output Block RAM **SHA CORE** writes final **hash**, 32-bit width PC reads through memory bus, 64-bit width, 133MHz ...

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A 1 Gbit/s partially unrolled architecture of hash functions SHA-1 and SHA-512

R Lien, T Grembowski, K Gaj - Lecture notes in computer science, 2004 - Springer

 ... cludes 32 4-kbit blocks of synchronous **dual**-ported RAM ... of the three FPGA devices was used to im- plement **hash core**. ... 8, the minimum clock periods of **SHA-1** and **SHA** ...

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Apparatus to Implement Dual Hash Algorithm

B Plessier - US Patent App. 10/531,843, 2002 - Google Patents

 ... further embodiment of the invention, a **dual hash** algorithm circuit ... Algorithm // High Level Algorithm initialize **SHA-1** internal ... 0] to W[15] start **core SHA-1** end ...

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Efficient single-chip implementation of SHA-384 and SHA-512

M McLoone, JV McCanny - 2002 IEEE International Conference on Field-Programmable ..., 2002 - ieeexplore.ieee.org

 ... The LUT was implemented using two **dual**-port Block RAMS (BRAMs) since ... 3] US NIST, Secure **Hash** Standard, Draft ... sha2S6-3X4-S12.pdf, 2001 [SI SECUCORE, **SHA-256 Core** ...

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•The IBM eServer z990 microprocessor

TJ Siegel, E Pfeffer, JA Magee - IBM Journal of Research and Development, 2004 - research.ibm.com

 ... the Data Encryption Standard (DES) and Secure **Hash** Algorithm (**SHA**) functions. ... on a single microprocessor chip; this is called a **dual-core** design point ...

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Dual processor trusted computing environment

CD Gressel, N Bayer, L Vichodets - US Patent App. 09/871,152, 2001 - Google Patents

 ... 13,2002 (54) **DUAL** PROCESSOR TRUSTED COMPUTING ENVIRONMENT (76) Inventors: Carmi David Gressel, Mobile Post Negev (IL); Nimrod Bayer, Beer Sheva (IL); Lev ...

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Security in embedded systems: Design challenges- [psu.edu](#) (PDF)

S Ravi, A Raghunathan, P Kocher, S Hattangady - ACM Transactions on Embedded Computing Systems (TECS), 2004 - portal.acm.org

 ... r **Hashing** algorithms such as MD5 and **SHA** provide ways of mapping mes- sages (with or without a key) into a fixed-length value, thereby providing "sig- natures ...

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Authentication engine architecture and method

M Buer, PY Law, Z Qi - US Patent App. 09/827,882, 2001 - Google Patents

 ... of the MD5 **hash** round logic and the **SHA1 hash** round logic ... is performed in parallel with the inner **hash** operation of ... A **dual**-frame input buffer is used for the ...

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Cali, efficient library for cache implementation

J Zola - Computer Science, 2004. ENC 2004. Proceedings of the Fifth ..., 2004 - [ieeexplore.ieee.org](#)

... All **core** elements are written using tem- plates and ... Every single node was **dual** AMD

Athlon 1600MHz with ... thanks to the application of the **SHA1 hashing** func- tion ...

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Authentication of data

F Yang, T Koskivirta, T Knuutila - US Patent App. 10/640,306, 2003 - Google Patents

... since it enables the **dual** functionality of ... applications can seamlessly integrate

hash and encryption ... than, for example, the corresponding **SHA**+AES combination. ...

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Key authors: [J Marchesini](#) - [S Smith](#) - [O Wild](#) - [A Raghunathan](#) - [R MacDonald](#)



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